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S5200D-TX

DIGITAL TEST TRANSMISSION TRANSMITTER

PRELIMINARY INSTRUCTION MANUAL

Form 0160-0131A

tau-tron

S5200D-TX

DIGITAL TEST TRANSMISSION TRANSMITTER

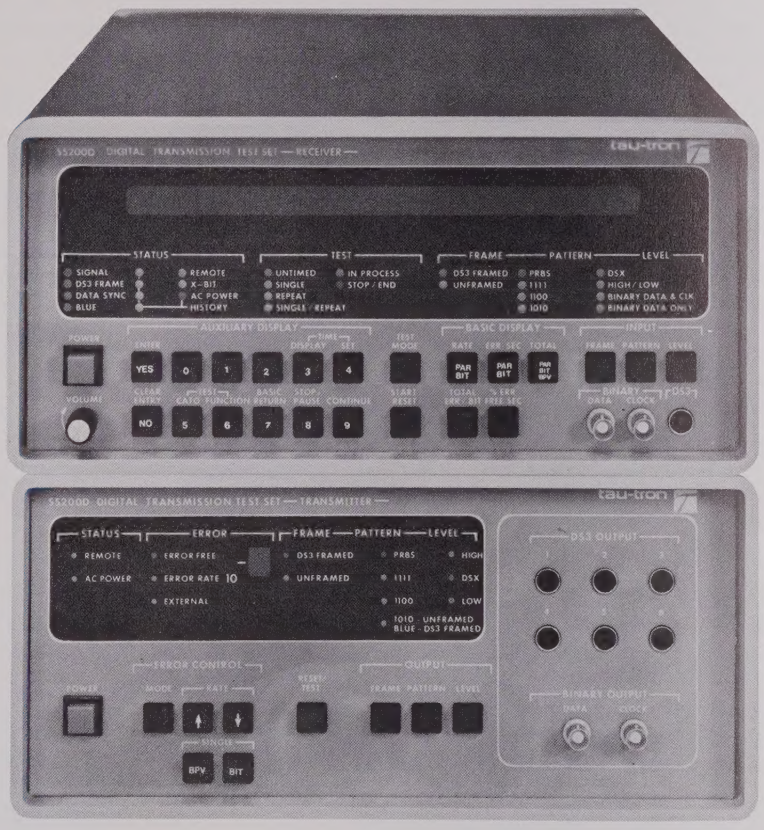
PRELIMINARY INSTRUCTION MANUAL

Form 0160-0181A

tau-tron

S5200D
Digital Transmission Test Set

- 11 basic measurements for system performance tests and characterization
- 24 additional records for fault analysis, monitoring, and statistical data
- Real-time information for correlation studies
- 32,767-bit DS3-compatible pseudorandom sequence, with or without framing
- Bipolar and binary-signal I/O testing, with or without clock
- Four different timing modes increases versatility
- Blue-signal generation, detection, and alarm
- Internal and external error injection in continuous or burst modes
- Extra-sensitive receiver works with greater than 23dB attenuation
- Easily read 40-character alpha-numeric display plus status indicators provide complete measurement data
- Optional RS232 output allows automatic, hard-copy records
- Mocroprocessor-based monitoring and analysis
- Ac and dc input power capability



For complete, Automatic Characterization of DS3 Transmission Systems

The Tau-Tron S5200D Digital Transmission Test Set is a compact test set for simple, yet flexible, measurements of systems operating at the DS3 transmission rate. It provides an unsurpassed degree of confidence in data collection and analysis for a wide variety of applications including commissioning, routine maintenance, troubleshooting, long-term monitoring and production testing of fiber optics, digital radio, digit multiplexers, and cable systems.

Flexible Sophistication

The S5200D's sophisticated microprocessor-based technology provides sufficient capabilities to characterize any common system and a few uncommon ones. Measurements and computations include the number of bit errors, parity violations, bipolar violations, bit and parity synchronous error-seconds, bit and parity error rates and average error rate, percent of error-free seconds, and tests for bit, parity, bipolar code, status, and alarm conditions. All measurements and computations are performed simultaneously.

A choice of test patterns allows a great deal of testing flexibility. A pseudorandom sequence of 32,767 bits, all ones, alternating 1100, and alternating 10, can all be generated. The all ones pattern without framing is a useful standard for calibrating signal levels. The unframed alternating 1100 and 10 patterns are useful for troubleshooting because they can be traced easily through a radio or fiber system and will be self-synchronizing on an oscilloscope. The alternating 10 pattern, when properly framed with the standard DS3 framing pattern, constitutes the "blue signal" to test the transmission system alarm circuitry. The test set

receiver automatically decodes this signal and provides both a front-panel indicator and rear-panel alarm signal output. Error injection can be manually controlled from 1 x 10^{-2} to 1 x 10^{-9} or externally controlled at continuous rates of from 5 to 450,000 errors per second or as bursts with variable duty cycles of error-free and error-conditioned signals to test systems stressed by various error conditions.

Exclusive Capabilities

The set operates not only with the standard B3ZS signal but with binary data and clock signals as well to adapt it to applications where B3ZS coding is not used. Operation with or without an external clock input is also possible. Because of its high sensitivity, the S5200D is guaranteed to work up to 450 feet downstream from a DSX cross-connect point and can be used with multiplexers or radios that attenuate the test signal by over 23 dB below the DS3 high level.

The S5200D is the only set of its kind that can generate the standard DS3-compatible 32,767-bit pseudorandom sequence with or without DS3 framing. The absence of framing allows measurements of switching-time faults in radio systems and the number of errors generated during a switch, and allows testing of satellite systems using unframed signals at the DS3 rate. Use of a pseudorandom sync pulse on both the transmitter and receiver permits measurements of variations in transit time in satellite patterns.

A new DS3 framing algorithm and fast-feed-forward data sync technique allows the set to acquire lock faster than other instrumentation and minimizes loss of sync in high-error-rate environments. This also allows measurements of reframe time in multiplexers, and allows investigations of the effects surrounding diversity and protection switches.

Complete, Concise Answers

A versatile, 40-character alpha-numeric display with large, easily read characters provides all data for the some 40 records the S5200D is capable of producing - from total bit errors to time of day.

The display, together with front-panel status indicators, are arranged so that two important characteristics can be displayed simultaneously for analysis. The combinations are all under total operator control.

Automatic, Unattended Operation

Long-term testing proceeds automatically and unattended because of several carefully considered design advantages - dc operation from office batteries in the event of an ac power failure, automatic circuits that measure the seconds the signals is lost, the frame is lost, data sync is lost, a blue signal is detected, and an X-bit is detected, and four external inputs that allow system or site parameters, such as alarms, to be logged in terms of seconds active during the test.

An audio output, with volume control, can be set to activate as a function of error rate, signal loss, frame loss, and blue-signal detection. This audible indication enables very fine system adjustments to be made in situations where the operator cannot see the test-set display.

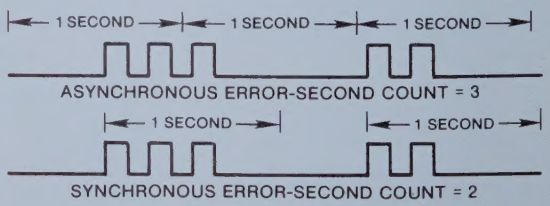
Equally important in many applications is an optional RS232 interface that permits connection of a printer to record all related events pertaining to each error-second, together with a periodic summary of important measured results, including the actual number of errors during the second, status information, etc.

Correlation Aids Trouble Analysis

Internal and external events can be correlated to error activity which greatly enhances the sets' ability to analyze complex problems. For example, the total parity errors can be measured while monitoring up to four external events and then correlating the activity of these parameters against the number of DS3 frame-losses or signal losses that may occur.

A Note About Error-Second Measurements

Two types of error-second measurements are in general use, asynchronous and synchronous.



With asynchronous measurements, contiguous one-second measurements are made starting at some time independent of the errors. Any error or errors occurring during any one-second interval registers as an error-second. With synchronous measurements, the one-second measurements are triggered by the errors.

Synchronous errored-second measurements always give the lowest possible count and always give consistent counts - two test sets making the same measurement will always read the same. For these reasons they are preferred by industry and are the type used by Tau-Tron.

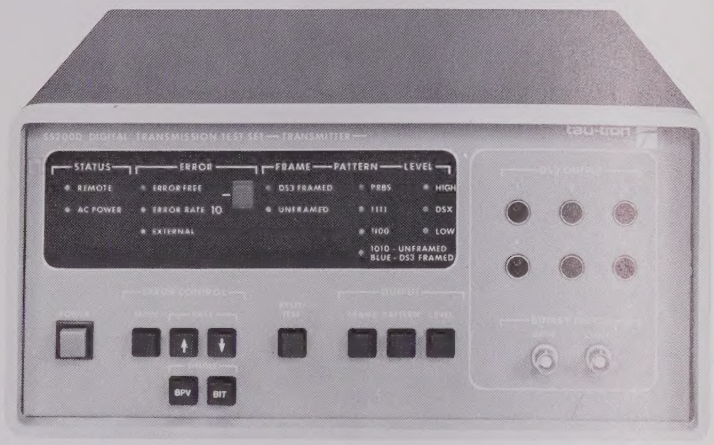
Everything you ever wanted to know about your DS3 Transmission Path but never had a system that could measure it all at one time, in one place, and at the push of a button, or two!

- Total Bit Errors
- Total Parity Errors
- Total Bipolar Violations
- Bit Error-Seconds
- Parity Error-Seconds
- Bit Error Rate
- Parity Error Rate
- Percent Bit Error-Free Seconds
- Percent Parity Error-Free Seconds
- Average Bit-Error Rate For Test Duration
- Average Parity-Error Rate For Test Duration
- Time of Day
- Time into Measurement
- Time Remaining in Measurement
- Bit Dribbling Error Rate
- Bit Dribbling Total Errors
- Bit Error-Seconds Where Rate Exceeds 10^{-3}
- Bit Error-Seconds Where Rate Exceeds 10^{-4}
- Bit Error-Seconds Where Rate Exceeds 10^{-5}
- Bit Error-Seconds Where Rate Exceeds 10^{-6}
- Parity Dribbling Error Rate
- Parity Dribbling Total Errors
- Parity Error-Seconds Where Rate Exceeds 10^{-4}
- Parity Error-Seconds Where Rate Exceeds 10^{-5}
- Parity Error-Seconds Where Rate Exceeds 10^{-6}
- Bipolar Error Rate
- Average Bipolar-Error Rate For Test Duration
- Percent Bipolar Error-Free Seconds
- Bipolar Error Seconds
- Number of Seconds During Which Lost Signal Was Detected
- Number of Seconds During Which Lost Frame Was Detected
- Number of Seconds During Which Lost Data Sync Was Detected
- Number of Seconds During Which X-Bit Was Detected
- Number of Seconds During Which Blue-Signal Was Detected
- Number of Seconds During Which Any of Four Different External Inputs Were Detected

TRANSMITTER SPECIFICATIONS (S5200D TX)

Clock: Clock can be internal, external, or externally jitter modulated. ***INTERNAL:*** 44.736MHz with stability of ±20ppm from 0 to 50°C. ***EXTERNAL:*** 44.736MHz ±0.5% at ECL compatible level into 75Ω ,ac coupled, applied to rear-panel BNC connector. When external clock input exceeds 500mV p-to-p, transmitter automatically switches to external clock.

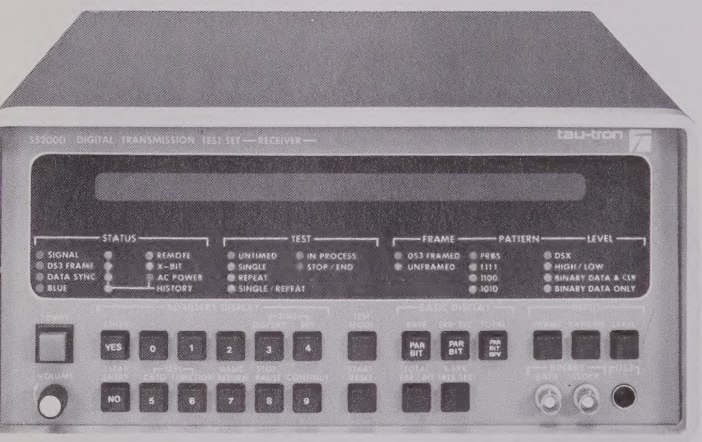
Data Patterns: Pattern and frame information indicated by front-panel LED's. ***PSEUDORANDOM:*** $2^{15}-1 = 32{,}767$ bit words, self-starting. ***SHORT WORDS:*** All one's (1111. . .), alternating 1100 (11001100. . .), and alternating 10(1010. . .). Alternating 10 pattern, when properly framed with the standard DS3 framing pattern constitutes a "blue signal". A logic-1 always follows each framing and control bit. ***FRAMED:*** Output is selected data pattern with standard Bell System DS3 frame and control bits added. ***UNFRAMED:*** Output is selected data pattern without any framing or control bits.



Status Monitor: A rear-panel 24-pin D connector provides normal and complemented TTL-compatible outputs for the pseudorandom sync pulse (one pulse per sequence), M sync pulse (from M1 to M2 in each frame), and ac power fail. An X-bit input is also provided that is held at a logic-1 whenever a blue signal is transmitted.

Error-Rate Injection: Bit or bipolar violations are injected into the output signal. Parity is computed on the data pattern prior to bit-error injections so parity errors will usually be generated. Bit errors or bipolar violations may occur in the framing as well as the data content. Bipolar violations are restricted to not occur in a B3ZS substitution, nor will they violate the B3ZS coding format so that bipolar error insertions will not cause bit errors. ***INTERNAL:*** 10^{-2} thru 10^{-9} bit-error insertion rate for integer values of the exponent; controlled by front-panel pushbuttons and indicated on front-panel readout. Single-bit or bipolar error inserted each time front-panel pushbutton is depressed. ***EXTERNAL:*** Applied to rear-panel BNC connector, TTL compatible, at rates from 5 to 450k errors/s, 220ns min pulse width. Allows any bit-error rate from 10^{-2} to 10^{-7}, as well as error bursts, to be transmitted, as set by rear-panel switch. Single bit-error injected each time input exceeds threshold thus causing transmitted bit-error rate to be a function of the input frequency in continuous mode. Burst errors (100%) are generated during the time the input exceeds threshold in burst mode.

Output: Outputs are DS3 and binary data and clock.



DS3: Available at 6 front-panel Weco 358 connectors with B3ZS code (bipolar three-zero substitution) at rate of 44.736 MHz, 11.2 ±1.1ns pulse at half amplitude, wih 4.5 ±1.5ns transition times. High level is 0.91V pk ±1.2 dB, DSX level includes insertion loss of 450 ft. of R/G728A cable, and low level of 13.8 ±2 dB below high-level (0.186V pk±2 dB) level is indicated on front-panel LED's. ***BINARY DATA:*** Available at front-panel BNC connector as binary NRZ with logic–1 of +1V and logic–0 of –1V with 75 Ω source impedance (other levels available, consult factory). ***BINARY CLOCK:*** Available at front-panel BNC connector as squarewave with logic–1 of +1V and logic–0 of –1V with 75Ω source impedance (other levels available, consult factory).

Power: ***AC POWER:*** 115V or 220V ±10%, 50 to 60 Hz, 70VA, via a 6-foot detachable power cord (supplied) that connects to a rear-panel receptacle and is stored in the cover when not in use. A front-panel AC FAIL LED indicator lights following restoration of power after a low-line or power-fail condition; indicator can be reset by front-panel pushbutton. ***DC POWER:*** –24V to –48V office power via a 6-foot detachable power cord (supplied) that connects to a rear-panel receptacle, separately fused. ***BACKUP:*** Internal battery provides backup power.

Mechanical: Portable bench-top blue-painted aluminum case with protective cover. Convenient carrying handle mounted on right side of case. ***DIMENSIONS:*** 6.6 in. high x 13.6 in. wide, x 19.82 in. deep overall including cover and handle. ***WEIGHT:*** 19 lbs. net, 24 lbs. shipping.

Accessories Supplied: Ac and dc power cords, protective cover, instruction manual, spare ac fuse, and spare dc fuse.

Option 01 Special Output Characteristics:
Binary data and clock output levels, other than +1V for logic–1 and –1V for logic–0 behind 75Ω at BNC connectors, can be provided; consult factory.

Option 02 IEEE-488 Interface: For remote control.

RECEIVER SPECIFICATIONS
(S5200D RX)

Input: Input can be DS3 at DSX or high/low-level or binary data with or without clock; input type indicated by front-panel LEDs. ***DS3:*** Applied to front-panel Weco 358 connector at rates up to 44.736 MHz; 75Ω input with return loss ≥20dB from 1 to 50 MHz. High/low range is 1.6V pk, 0.91V nominal for high signal; 13.8 dB below high for low signals; 11.2 ±1.1ns pulse at half amplitude, with 4.5 ±1.5ns transition times and <10% overshoot/undershoot. DSX level includes insertion loss of a cable equalizer that equalizes 450 to 900 ft. of R/G728A cable. Low level sensitivity sufficient for insertion losses ≥23dB. ***BINARY DATA*** input is binary NRZ of 500mV p-to-p amplitude, OV threshold, 75Ω (other levels available, consult factory). ***BINARY CLOCK*** input is squarewave of 500mV p-to-p amplitude, OV threshold, 75Ω (other levels available, consult factory).

Data Patterns: ***PSEUDORANDOM:*** $2^{15}-1$ = 32,767 bits per word. ***SHORT WORDS:*** All one's (1111...), alternating 1100 (11001100...), alternating 10 (1010...). Alternating 10 pattern, when properly framed with the standard DS3 framing pattern, constitutes a "blue signal".

Error Determination: ***BIT ERROR:*** Framed or unframed. Inequality between received data pattern and receiver's internally generated data pattern. ***PARITY ERROR:*** Framed only. Inequality between the parity bit calculated from live-traffic data bits or test-pattern data bits with the actual received parity bit in its usual position in the next frame. ***BIPOLAR ERROR:*** Framed or unframed. Bipolar violations detected on live traffic or test patterns.

Timing Modes: One of four timing modes can be pushbutton selected, a front-panel LED indicates the mode in use: ***UNTIMED:*** (Default, power-up mode). Continuous indication of accumulated errors and elapsed time. ***SINGLE:*** Errors are accumulated over a period of time from 1 second to 99 days as selected by front-panel pushbuttons. ***REPEAT:*** Same as Single except at the end of each test time the results are cleared and a new test is started; data displayed is from last test completed. ***SINGLE/REPEAT:*** A combination of Single and Repeat where the single duration time is longer than the repeat time; data displayed is from last test completed. Useful for long-term tests or any test where data would be printed automatically (Repeat Interval) over a long-term period.

Basic Error Measurements: These measurements can be made in any of the four timing modes (above). ***TOTAL:*** Bit and parity errors and bipolar violations are measured simultaneously; displayed separately. ***ERROR SEC:*** Bit and parity errors are

measured simultaneously; displayed separately. ***ERROR RATE:*** Bit and parity errors are measured simultaneously; displayed separately. Timebase is 10^8 bits (approx. 2.2s) in Untimed or Single mode, operator selected in Repeat mode or Single/Repeat Mode. ***AVERAGE BIT ERROR RATE:*** Total error count divided by total bits accumulated since start of test (last Reset); displayed as long as associated front-panel pushbutton is depressed. ***PERCENT ERROR FREE SEC:*** Percent of error-free seconds since start of test (last Reset); displayed as long as associated pushbutton is depressed.

Auxiliary Measurements: These measurements can be made in any one of the four timing modes (above). ***BIT DRIBBLING ERROR RATE:*** The bit error rate that remains after subtraction of all errors during error seconds where the error rate was greater than 1×10^{-6}. ***TOTAL DRIBBLING BIT ERRORS:*** Total number of bit errors that remain after subtraction of all errors during error seconds where the error rate was greater than 1×10^{-6}. ***BIT THRESHOLD ERROR SECONDS:*** Bit error rate that exceeds threshold of 10^{-3}, 10^{-4}, 10^{-5}, and 10^{-6}; measured simultaneously and selected individually for display by front-panel pushbuttons. ***PARITY DRIBBLING ERROR RATE:*** The parity error rate that remains after subtraction of all errors during error seconds where the error rate was greater than 1×10^{-6}. ***TOTAL DRIBBLING PARITY ERRORS:*** Total number of parity errors that remain after subtraction of all errors during error seconds where the error rate was greater than 1×10^{-6}. ***PARITY THRESHOLD ERROR SECONDS:*** Parity error rate that exceeds thresholds of 10^{-4}, 10^{-5}, and 10^{-6}; measured simultaneously and selected individually for display by front-panel pushbuttons. ***BIPOLAR ERROR RATE, ERROR SECONDS, AVERAGE ERROR RATE, and PERCENT ERROR-FREE SECONDS.***

Clock: Built-in real-time clocks are used for time of day, time-into-test, time-remaining-in-test, and time of all status and alarm conditions; any of which can be displayed on the display, as selected by the operator. Time can be set by front-panel pushbuttons.

Display: 40-character high-brightness alpha-numeric with 0.235-in. high 5 x 7 dot-matrix characters. Full display used for operator prompting when setting initial measurement conditions; divided into a right and left field for simultaneous indication of two measured values, user selected; both with appropriate user-oriented names for unambiguous readouts.

Simultaneous Displays

Left Field	Right Field
Basic Error Measurements: Bit error-seconds (7 digits plus overflow), parity error-seconds (7 digits plus overflow), bit error rate (2 digits with 2-digit exponent).	**Basic Error Measurements:** Total bit errors (9 digits plus overflow), total parity errors (9 digits plus overflow), total bipolar violations (9 digits plus overflow).
Basic Error Measurements: Percent bit error-free seconds (7 digits), Percent parity error-free seconds (7 digits), total bit errors/total bits (2 digits with 2-digit exponent), total parity errors/total bits (2 digits with 2-digit exponent).	**Clock:** Time into measurement up to 99 days, 23 hours, 59 minutes, 59 seconds.
Auxiliary Measurements: Bit dribbling error rate (2 digits with 2-digit exponent), total bit dribbling errors (7 digits plus overflow), bit threshold error seconds with thresholds of 10^{-3}, 10^{-4}, 10^{-5}, or 10^{-6} (7 digits plus overflow), parity dribbling error rate (2 digits with 2-digit exponent), total parity dribbling errors (7 digits plus overflow), parity threshold error seconds with thresholds of 10^{-4}, 10^{-5}, or 10^{-6} (7 digits plus overflow), bipolar error rate (2 digits with overflow), bipolar error seconds (7 digits plus overflow), bipolar average error rate (7 digits plus overflow), and percent bipolar error-free seconds (7 digits).	**Basic Error Measurements:** Total bit errors (9 digits plus overflow), total parity errors (9 digits plus overflow), total bipolar violations (9 digits plus overflow), total bipolar violations (9 digits plus overflow).
Status and Alarm: All values are seconds during which condition occurred, 7 digits plus overflow: signal loss, frame loss, data sync loss, blue-signal detected, X-bit detected and external-event A, B, C, and D inputs detected.	

Clock: Time-of-day, elapsed time, elapsed time and time remaining in single test, test duration set for single test, elapsed time and time remaining in repeat test, test duration set for repeat test.

Status and Alarm: The following conditions are indicatd by front-panel LED indicators, by the front-panel display together with the number of seconds during which each occurred and/or by an audible alarm at the operator's discretion. Another front-panel LED indicates when the transmitter is under remote control. (see Option 02 IEEE-488 Interface, below).

Condition	Display (seconds)	Status LED	History LED	Audible Alarm
Signal Loss	X	X	X	X
Frame Loss	X	X	X	X
Data Sync Loss	X	X	X	
Blue-Signal Detected	X	X	X	X
X-Bit Detected	X	X		
Ac-Power Loss		X	X	
Remote-Control		X		
External A, B, C, D Event Detected				
Error Rate Excessive				X

AUDIBLE ALARM: In addition to responding to the status conditions selected by the operator, the audible alarm can be selected to respond to the error rate, with the audio output proportional to the rate of errors counted. Volume is set by a front-panel control.

Status Monitor: A rear-panel 24-pin D connector provides normal and complemented TTL-compatible outputs for the pseudorandom sync pulse (one pulse per sequence), blue-pattern detected, X-bit detected (when framing is used), signal loss, DS3 frame loss, data-sync loss, and status alarm. Four TTL compatible inputs are also provided (A, B, C, D) for counting and display as event seconds.

Signal Monitors: Five separate rear-panel BNC connectors provide output signals behind 75 Ω for recovered clock (±0.5V), bit error (±0.5V, RZ format), bipolar errors (±0.5V, RZ format), parity error (TTL compatible, RZ format), and M-sync (TTL compatible from M1 to M2 in each frame).

Power: ***AC POWER:*** 115V or 220V ±10%, 50 to 60 Hz, 100VA, via a 6-foot detachable power cord (supplied) that connects to a rear-panel receptacle and is stored in the cover when not in use. AC FAIL LED indicator lights following restoration of power after a low-line or power-fail condition; indicator can be reset by front-panel pushbutton. ***DC POWER:*** -24V to -48V office power via a 6-foot detachable power cord (supplied) that connects to a rear-panel receptacle, separately fused. ***BACKUP:*** Internal battery provides backup power.

Mechanical: Portable bench-top blue-painted aluminum case with protective cover. Convenient carrying handle mounted on right side of case. ***DIMENSIONS:*** 6.6 in. high x 13.6 in. wide x 19.82 in. deep overall including cover and handle. ***WEIGHT:*** 21 lbs. net, 26 lbs. shipping.

Accessories Supplied: Ac and dc power cords, protective cover, instruction manual, spare ac fuse, and spare dc fuse.

Option 01 Special Input Characteristics: Binary data and clock input levels, other than +1V for logic-1 and -1V logic-0 into 75 Ω at BNC connectors, can be provided; consult factory.

Option 02 IEEE-488 Interface: For remote control, front-panel LED indicates when receiver is under remote control.

Option 03 RS232 Interface: For output to printer, analog modem, or auxiliary channel. Printouts are made at the end of an error-second and at the end of a test. ***END OF ERROR SECOND:*** Real time at the end of the error-second, errors accumulated during the error-second, and the event seconds for signal loss, frame loss, data sync loss, blue-signal detected, X-bit detected, and external A, B, C and D inputs. ***END OF TEST:*** Real time, accumulated total errors, accumulated error-seconds, and dribbling error rate.

S5200D-TX Digital Transmission Test Transmitter

OPTIONS for added capability:
- OP-01 Special Output Characteristics
- OP-02 IEEE-488 Interface
- OP-03 RS232 Interface

S5200D-RX Digital Transmission Test Receiver

OPTIONS for added capability:
- OP-01 Special Input Characteristics
- OP-02 IEEE-488 Interface
- OP-03 RS232 Interface

Specifications are subject to change without notice.

tau-tron

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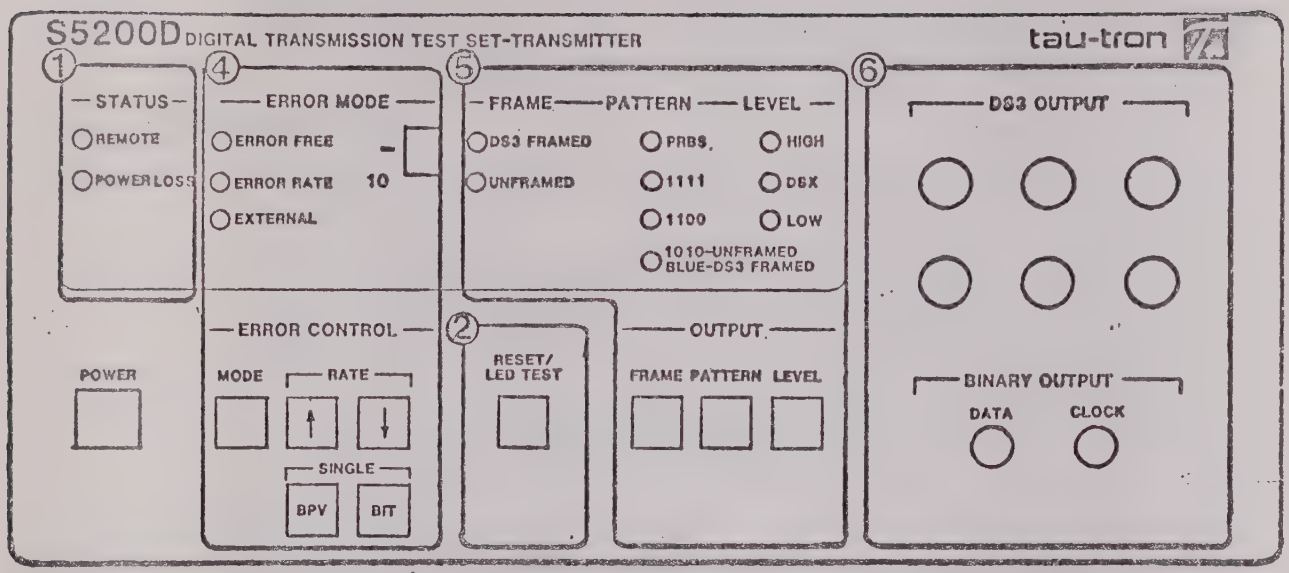
Form 138-980C



Multi-selection pushbuttons — Several pushbuttons are multi-selection; that is, each time they are pushed they select a different operating characteristic and then return to the initial characteristic in the sequence. For example, by repetitively pushing the MODE button, you can select error free, internal error injection, or external error inject modes. Pushing the MODE button after the last choice (external error inject) has been selected will return the mode to the first choice in the sequence (error free).

Indicator lights — Green....Normal condition
Yellow...Special condition
Red.....Alarm

STEP 1 STATUS

Control	Selection	Notes
None. Indicator signifies status of remote control input	Control by external input	REMOTE yellow indicator signifies unit is under remote control by IEEE 488 or RS-232 input applied to rear-panel connector.
None. Indicator signifies status of ac power.	AC power lost	AC POWER yellow indicator signifies ac power input was lost for some time during test.

STEP 2 TEST

Control	Selection	Notes
RESET/TEST	Reset AC POWER LED, test indicators	PUSH to reset AC POWER LED and to light all front-panel indicators.

STEP 3 CLOCK SOURCE

Internal	The normal operation is with an internal clock source of 44.736 MHz (DS3 rate).
External	If an external signal of 44.736 MHz ±2% is connected to the EXT CLOCK in rear-panel BNC connector, and if the signal exceeds 500mV p-to-p, the transmitter automatically switches to external clock.
Jitter	The external clock signal can be modulated to provide jitter. A JITTER INJECT rear-panel BNC connector is provided for possible future use but is presently not wired.

STEP 4 ERROR INJECTION

Control	Selection	Notes
MODE	Error free	ERROR FREE green indicator light.
	Error rate	ERROR RATE yellow indicator light.
(RATE ↑) (RATE ↓)		Push RATE ↑ to increase error rate, RATE ↓ to decrease it; as indicated on display from 10^{-2} thru 10^{-9}. Display is dim in Error-free mode to indicate the rate that would be selected in Error-rate mode; display is bright in Error-rate mode.
	External	EXTERNAL yellow indicator light. Apply signal to ERROR INJECT rear-panel BNC connector. For triggered errors (error injected each time input exceeds threshold) set toggle switch to RATE. For burst errors (100% error injection during time input exceeds threshold) set toggle switch to BURST.
SINGLE BPV	Single bipolar error	Push SINGLE BPV to inject a single bipolar error in Error-free mode.
SINGLE BIT	Single bit error	Push SINGLE BIT to inject a single bit error in Error-free mode.

STEP 5 OUTPUT SELECTION

Control	Selection	Notes
FRAME	DS3 framed	DS3 FRAMED green indicator light. If parity tests are to be made, output must be set for framed signal.
	Unframed	UNFRAMED yellow indicator light.
PATTERN	Pseudorandom	PRBS green indicator light.
	All one's Alternating 1100 Alternating 10	111,1100, or 1010 yellow indicator light; depending on setting of rear-panel toggle switch.
LEVEL	High	HIGH yellow indicator light.
	DSX	DSX green indicator light.
	Low	LOW yellow indicator light.

STEP 6 OUTPUT CONNECTION

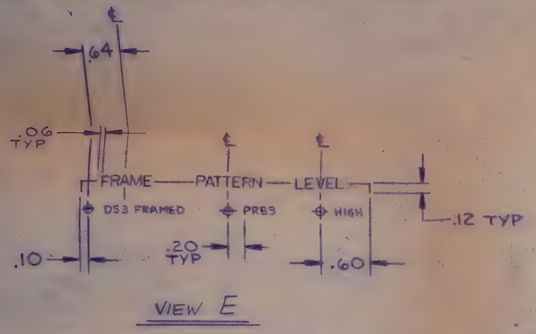
Binary data only	Connect 75Ω cable from Binary Output DATA BNC connector to system under test.
Binary data with clock	Connect 75Ω cables from Binary Output DATA and CLOCK BNC connector to system under test.
DS3	Connect 75Ω cable from any of the DS3 OUTPUT WeCo 358 connectors to system under test.

STATUS MONITOR

A rear-panel 24-pin D connector provides six TTL compatible outputs and one TTL compatible input.

Pin	I/O	Active	Max Sink	Function
7	output	high	40mA	M sync pulse
18	output	low	40mA	M sync pulse′
17	output	high	40mA	PR sync pulse
5	output	low	40mA	PR sync pulse′
10	output	high	40mA	Lost power
22	output	low	40mA	Lost power′
21	input	---	---	X-bit; low-level in sets X-bit low, high-level in or no connection sets X-bit high
11,12,14	---	---	---	Ground
23,24	---	---	---	Ground

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	ADD NEXT ASSY Nº		
	2	UPDATE PER PROTOTYPE	2-26-80	
	A	REL TO PROD	8-26-80	
	B	REVISED PER DCN 00824	12-18-80	



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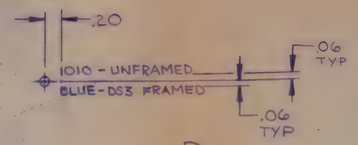
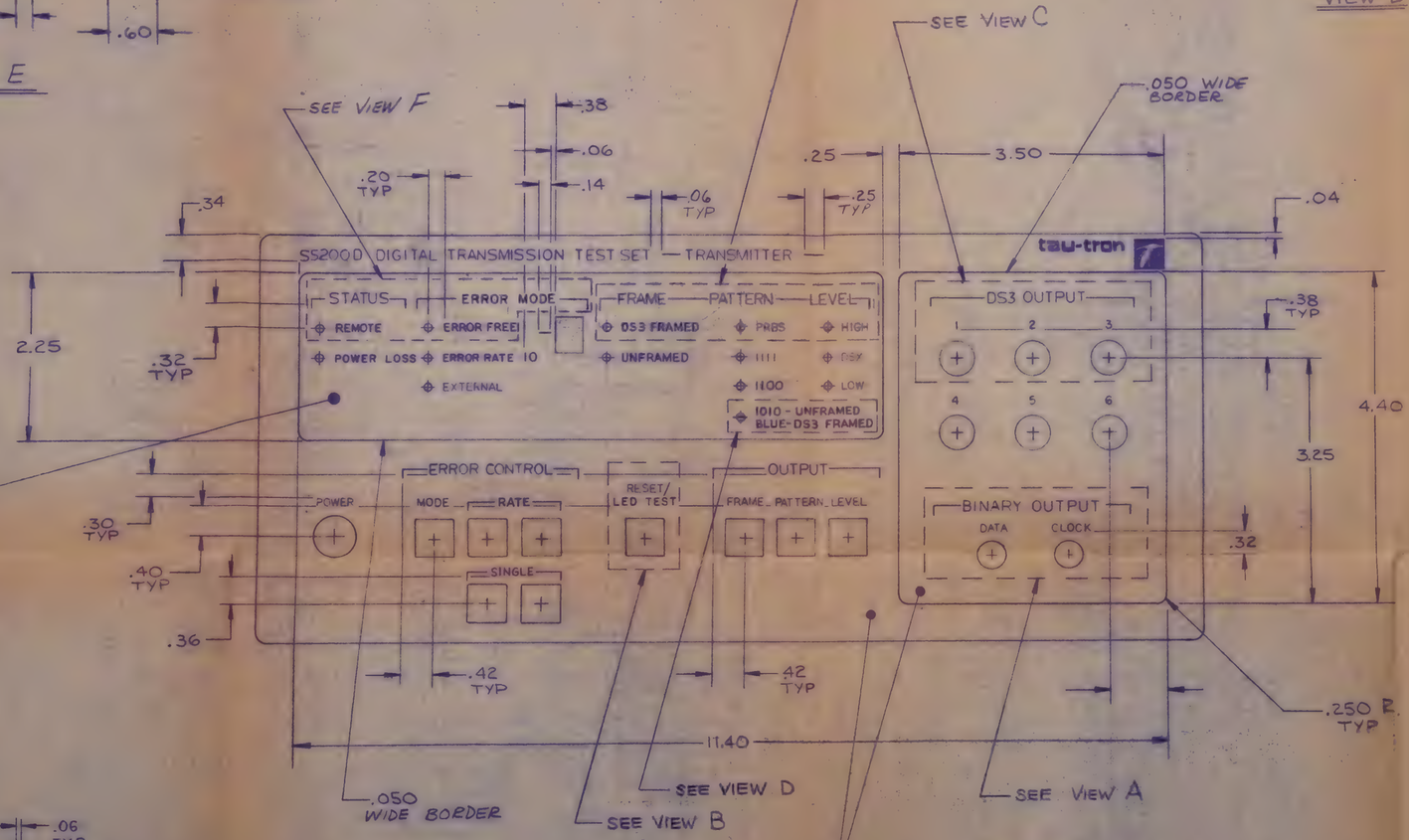
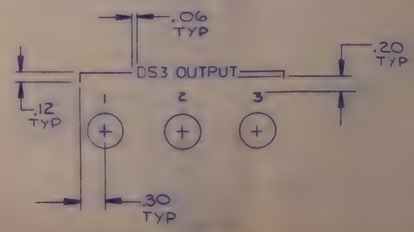
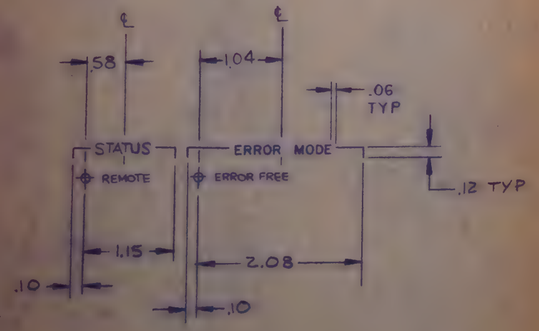


VIEW D

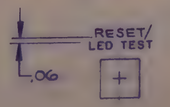




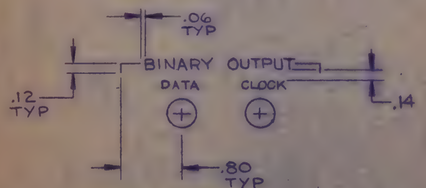
VIEW C



VIEW F



VIEW B



VIEW A

CHARACTER LEGEND	SIZE & TYPE
tau-tron	.16 PT. DEMI-BOLD
S5200D, DIGITAL, TRANSMISSION, TESTSET, TRANSMITTER, STATUS, ERROR MODE, PATTERN, LEVEL, DS3 OUTPUT, FRAME, ERROR CONTROL, OUTPUT, BINARY OUTPUT, IO	.12 PT. DEMI-BOLD
ALL REMAINING CHARACTERS	.10 PT. DEMI-BOLD
INDICATOR LINES	.030 WIDE

NOTES:
1. CHARACTERS & INDICATOR LINES TO BE LOCATED CENTERED IN RESECT TO THEIR OWN MACHINE HOLES, CUTOUTS & BOX LINES UNLESS NOTED
2. ALL CHARACTERS AND INDICATOR LINES TO BE PAINTED WHITE
3. PAINT LIGHT BLUE PER 25190
4. REF MACHINE DWG. TDG-57153

WHERE APPLICABLE: REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

TDH-57155	XMTR S5200D
NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± .010
2 PLACE DECIMALS ± .02
1 PLACE DECIMALS ±
MATERIAL:

CONTR NO.

DR	M. COSTELLO	7APR80
CHK		
APPD		8-26-80
APPD		9-2-80

APPROVED
BY DIRECTION OF

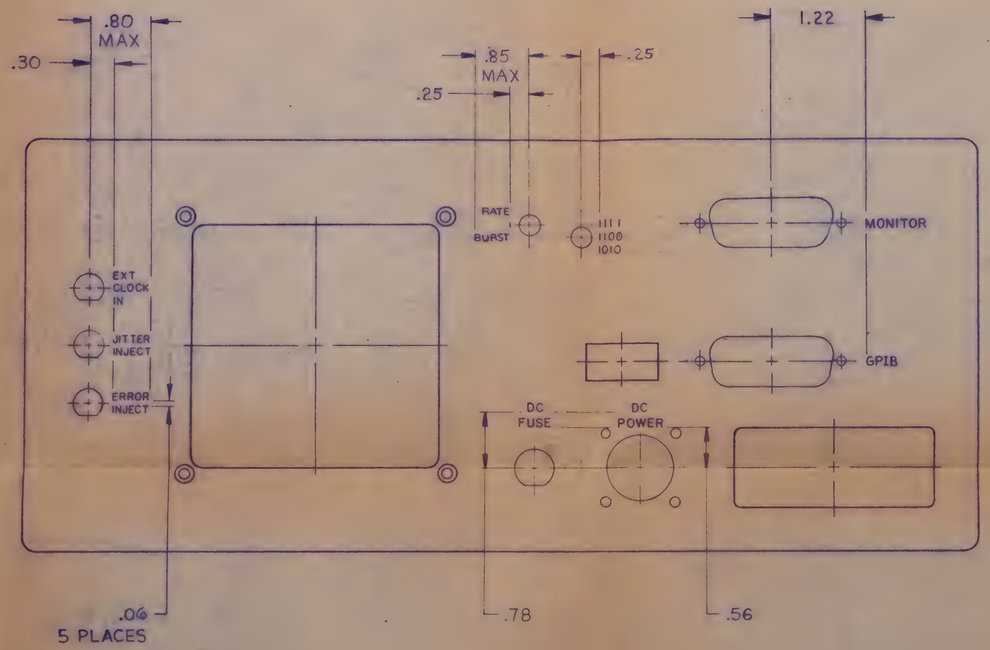
tau-tron INC Chelmsford, Ma. 01824

DRAWING TITLE
FRONT PANEL SCREEN TRANSMITTER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		TDH-57099	B

SCALE 1/1 | S5200 D | SHEET

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REL TO PROD	8-26-80	
	B	REVISED PER DCN00748	9-29-80	
	C	REVISED PER DCN00772	10-23-80	
	D	REVISED PER DCN00824	11-7-80	



NOTES:

1. CHARACTERS TO BE CENTERED AND LOCATED IN RESPECT TO THEIR OWN MACHINE HOLES AND CUTOUTS UNLESS NOTED
2. PAINT NEARSIDE WITH FED STD 595A LIGHT BLUE #25190, SMOOTH FINISH
3. ALL CHARACTERS PAINTED WHITE
4. REF MACHINE DWG TDG-57133

CHARACTER LEGEND	SIZE & TYPE
EXT, CLOCK, IN, JITTER ERROR, INJECT	10 POINT DEMI-BOLD
RATE, BURST, 1111, 1100 1010	8 POINT MEDIUM
DC POWER, DC FUSE, GPIB, MONITOR	12 POINT DEMI-BOLD

WHERE APPLICABLE:
REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

TDH-57134	S5200D TX
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± —
2 PLACE DECIMALS ± .02
1 PLACE DECIMALS ± —
MATERIAL: —

CONTR NO.

DR KRW	28APR80
CHK	28 APR 80
APPD	2-2-80
	7-2-80

APPROVED
BY DIRECTION OF

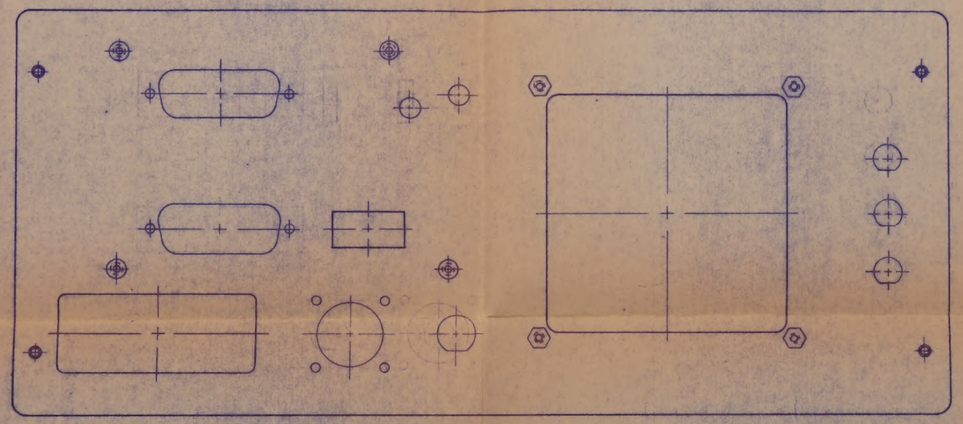
tau-tron inc
Chelmsford, ma. 01824

DRAWING TITLE
REAR PANEL, TRANSMITTER, SCREEN

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		TDH-57135	D

SCALE — SHEET

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	REV PER DCN 00824 JRP	1-12-81	BRC



WHERE APPLICABLE:
REMOVE ALL BURRS & BREAK SHARP EDGES TO 1/64.

TDH-57159	SS200D TX
NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± —
FRACTIONS ± —
3 PLACE DECIMALS ± —
2 PLACE DECIMALS ± —
1 PLACE DECIMALS ± —

MATERIAL: —

CONTR NO.

DR	JRP	28 APR 80
CHK		
APPD		8-26-80
		1-2-80

APPROVED

BY DIRECTION OF

tau-tron inc
Chelmsford, mass. 01824

DRAWING TITLE
REAR PANEL, TRANSMITTER SCREEN

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		TDH-57135	D

SCALE: 1/1 | SS200D | SHEET 2 OF 2

27 Industrial Avenue, Chelmsford, MA 01824 (617) 256-9013